REMARKS

The present Amendment is in response to the Official Action of February, 27, 2003, in which Claims 1, 2, and 4 are rejected. Applicants have thoroughly reviewed the outstanding Office Action including the Examiner's Actions and the references cited therein. The following remarks are believed to be fully responsive to the Office Action and, when coupled with the present invention, are believed to render all claims at issue patentably distinguishable over the cited references.

No Claims are cancelled herein. Claim 13 is added and Claims 1, 2, and 4 are amended herein.

Applicants respectfully request reconsideration in light of the following remarks.

DRAWINGS ISSUE

With respect to Page 2 of the Office Action, the Drawings are objected to due to improper crosshatching and no label for the claimed "second plating through holes".

Applicants respectfully traverse these rejections.

Applicants have amended the Figures 3 through 7 and added label --40-- to the "second conductive holes" claimed in amended Claim 1 and new Claim 13. All changes are in accordance with the specification as originally filed and no new matter is entered.

CLAIM OBJECTIONS ISSUE

With respect to Page 3 of the Office Action, the Examiner rejected Claims 2 and 4 because of informalities.

Applicants have amended the informalities in Claims 2 and 4. Accordingly, Applicants respectfully traverse these rejections.

CLAIM REJECTIONS – 35 U.S.C. SECTION 112

With respect to Page 2 of the Office Action, the Examiner rejected Claims 1, 2 and 4 under 35 U.S.C. 112.

Applicants respectfully traverse these rejections.

Applicants cancel the recitation "and via said first insulating layer" and amend the recitation --having a plurality of first conductive holes therein—in independent Claim 1, and the added recitation --a sidewall connecting said back surface and said active surface-- to independent Claim 1, and the added recitation --said back surface and said sidewall are affixed to said cavity-- to independent Claim 1.

Furthermore, for clarity and in accordance with Figures 3 through 7, Applicants cancel the recitation "or combination of above" and add the recitation – and both above said chip and above surrounding of said chip—to the dependent Claim 4. These amendments are in accordance with the specification and drawings as originally filed and no new matter is entered.

CLAIM REJECTIONS – 35 U.S.C. SECTION 102(b)

With respect to Page 3 through Page 5 of the Office Action, the Examiner rejected Claims 1, 2, and 4 as being unpatentable over Malladi.

Examiner is of the opinion that Malladi discloses a semiconductor device as claimed in the invention.

Applicants respectfully traverse these rejections.

Initially, Malladi discloses an integrated circuit package that has an integrated circuit die having a second face bearing a plurality of first electrical contacts, a substrate including a plurality of second contacts disposed along a first surface thereof mating coupled to the plurality of first electrical contacts, and an auxiliary circuit device located within the inner chamber defined by a compartment of the substrate (claims 1 and 15). Malladi also teaches a cap 100 having a top 102 and a perimeter lip 104 to define a sealed chamber 106 containing the die, the underside 108 of the cap 100 **forming a pressuring surface engaging the upper face 22 of the die** (col. 4, lines 17-24), and **an epoxy-type encapsulation material 31 secures the die to the substrate** (col. 3, lines 24-26). Furthermore, an array of solder bumps 40 connects each contact 28 of the die 20 with an associated contact 38 of the substrate (col. 3, lines 38-40). Accordingly, Malladi teaches a cap 100 having a chamber containing the die, and the cap and the die are **in a spaced-existing relation** and attached to each other **with only the upper face of the die**. Further, **the substrate is affixed to the die with the solder bumps**.

However, the amended Claims of the Invention emphasize the carrier having a cavity **configured for fitting a chip**, and **the back surface and the sidewall** of the chip are attached to the cavity (amended Claim 1 and new Claim 13, and Page 6, lines 5 through 8 in the Specification as originally filed). Thus, the relationship between cavity and chip taught by the Invention differs from the one between the cap and the die taught by Malladi.

Furthermore, the instant claims emphasize **the first insulating layer on both the chip and the carrier**, and the first conductive holes in the first insulating layer corresponding to the bonding pads of the chip (Claim 1), and Page 6, lines 8 through 10 in the Specification as originally filed). Moreover, **the first insulating layer would provide protection and planarization for the chip and the carrier** (Page 6, lines 13 through 15 in the Specification as originally filed). Accordingly, **there are no solder bumps between chip and substrate in the Invention,** which differs from the solder bumps taught by Malladi.

On the other hand, it is not necessary for the Invention to have an auxiliary circuit device located within the inner chamber of the substrate, thus, **the distribution of solder balls taught by the Invention would be on the surrounding of the chip, or above the chip, or both** (FIGS. 3 and 6, Page 7, lines 23 through 24). However, the auxiliary circuit taught by Malladi restricts the distribution of the solder balls 52. Accordingly, the multi-layer taught by the Invention differs from the substrate taught by Malladi.

Accordingly, it is respectfully submitted that Claims 1, 2, 4 and 13 as currently presented are patentable over the cited art. Specifically, it is believed that these claims are patentable over Malladi.

Reconsideration and withdrawal of these rejections are respectfully requested.

MARKED-UP CHANGES

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached paper is captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE**".

CONCLUSION

In light of the above amendments and remarks, Applicants respectfully submit that all pending Claims 1 , 2, 4 and 13 as currently presented are in condition for allowance. Accordingly, reconsideration is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

The paragraph beginning at page 2, line 15:

It is another object of the present invention to provide improved structure of FCBGA and manufacture thereof. The redistribution and solder-bump process for a conventional structure of FCBGA are simplified and integrated into the fan-out process of build-up substrate.

The paragraph beginning at page 2, line 26:

In the present invention, a semiconductor packaging device ~~comprises~~ has a carrier having at least a cavity or a slot thereon for fitting at least a chip. ~~At least a~~ The chip has a back surface ~~and~~, an active surface with a plurality of first bonding pads, and a sidewall connecting the back surface and the active surface. The back surface and the sidewall of the chip ~~is~~ are affixed to the cavity ~~to~~ and expose the active surface. A first insulating layer is coated on both the active surface and the carrier, ~~which comprises~~ and has first ~~plating through~~ conductive holes therein. The first conductive holes are corresponding ~~connected~~ to first bonding pads ~~and via the first insulating layer~~. A multi-layer structure is on the first insulating layer, which ~~comprises~~ has conductive layout lines, second ~~plating through~~ conductive holes therein, ~~and~~ a second insulating layer thereon and exposed ball pads ~~thereon~~ in the second insulating layer. The first ~~plating through~~ conductive holes are electrically connected with the conductive layout lines, the second ~~plating through~~ conductive holes, and the exposed ball pads. A plurality of solder balls are affixed to the ball pads. Such architecture integrates the redistribution and fan-out process, which simplifies the conventional process for flip-chip ball grid array.

The paragraph beginning at page 5, line 8:

In the present invention, a semiconductor packaging device ~~comprises~~ has a carrier having at least a cavity or a slot thereon for fitting at least a chip. ~~At least a~~ The chip has a back surface ~~and~~, an active surface with a plurality of first bonding pads, and a sidewall connecting the back surface and the active surface. The back surface and the sidewall of the chip ~~is~~ are affixed to the cavity ~~to~~ and expose the active surface. A first insulating layer is coated on both the active surface and the carrier, ~~which comprises~~ and has first ~~plating through~~ conductive holes therein. The first conductive holes are corresponding ~~connected~~ to first bonding pads ~~and~~

~~via the first insulating layer~~. A multi-layer structure is on the first insulating layer, which ~~comprises~~ has conductive layout lines, second ~~plating through~~ conductive holes therein, ~~and~~ a second insulating layer thereon and exposed ball pads ~~thereon~~ in the second insulating layer. The first ~~plating through~~ conductive holes are electrically connected with the conductive layout lines, the second ~~plating through~~ conductive holes, and the exposed ball pads. A plurality of solder balls are affixed to the ball pads. Such architecture integrates the redistribution and fan-out process, which simplifies the conventional process for flip-chip ball grid array.

The paragraph beginning at page 7, line 22:

FIGS. 3-5 are cross-sectional views illustrating the packaging chip cut with line 2A-2A of FIG. 2. Depicted in FIG. 3, solder balls are distributed on the surrounding of the chip. After the chip 20 is placed in the carrier 11 and affixed by an adhesive 19, an insulating layer 14 is formed on the active surface 30 of the chip 20 and the carrier 11 where the bonding pads 21 of the chip 20 are exposed. Multitudes of plating through 22 in the insulating layer 14 are corresponding and electrically connected to the bonding pads 21. A multi-layer film 15 with predetermined circuit 23 and plating through holes ~~22~~ 40 is on the insulating layer 14 and thereafter another insulating layer 16 is formed on the multi-layer film 15 only to expose the pads 18 of the plating through holes ~~22~~ 40 on which the solder balls 17 are affixed, and the solder balls are distributed on the carrier 11, the chip 20, or both. Thus, the pad redistribution, bumping, and fan-out processes for the chips can be implemented at ~~one time~~ same process. One of advantages of the present invention is to avoid the direct chip attachment to a print circuit board for fear of poor reliability. Furthermore, the packaging thickness is minimum and the heat radiation is improved.

In the Claims:

1. A semiconductor packaging device comprising:

a carrier having at least a cavity thereon, said cavity configured for fitting a chip;

~~at least a~~ said chip having a back surface ~~and~~, an active surface, and a sidewall connecting said back surface and said active surface, wherein said ~~chip is~~ back surface and said sidewall are affixed to said cavity ~~to~~ and exposed said active surface, and said active surface has a plurality of first bonding pads;

a first insulating layer coated on said active surface and said carrier~~, said first insulating layer comprising~~ and having a plurality of first ~~plating through~~ conductive holes therein, wherein said first conductive holes correspond ~~connected~~ to first bonding pads ~~and via said first insulating layer~~;

a multi-layer structure on said first insulating layer, said multi-layer structure ~~comprising~~ having a plurality of conductive layout lines, a plurality of second ~~plating through~~ conductive holes therein, ~~and~~ a second insulating layer thereon, and a plurality of exposed ball pads ~~thereon~~ in said second insulating layer, wherein said first ~~plating through~~ conductive holes are electrically connected with said conductive layout lines, said second ~~plating through~~ conductive holes, and said exposed ball pads; and

a plurality of solder balls affixed to said exposed ball pads.

2. The semiconductor packaging device of claim 1, wherein said carrier is made of a material selected from groups consisting of a silicon substrate, a ceramic substrate, a glass substrate, an organic substrate, or combination of above.

4. The semiconductor packaging device of claim 1, wherein said ball pads are distributed at a location selected from the groups consisting of above said chip, above surrounding of said chip, ~~or combination of above~~ and both above said chip and above surrounding of said chip.

13. A semiconductor packaging device comprising:

a carrier having at least a cavity thereon, said cavity configured for fitting a chip;

said chip having a back surface, an active surface, and a sidewall connecting said back surface and said active surface, wherein said active surface has a plurality of first bonding pads;

an adhesive affixing said back surface and said sidewall to said cavity;

a first insulating layer coated on said active surface and said carrier and having a plurality of first conductive holes therein, wherein said first conductive holes correspond to first bonding pads;

a multi-layer structure on said first insulating layer, said multi-layer structure having a plurality of conductive layout lines, a plurality of second conductive holes therein, a second insulating layer thereon, and a plurality of exposed ball pads in said second insulating layer, wherein said first conductive holes are electrically connected with said conductive layout lines, said second conductive holes, and said exposed ball pads; and

a plurality of solder balls affixed to said exposed ball pads.

In the Abstract:

A semiconductor packaging device ~~comprises~~ has a carrier having ~~at least~~ a cavity ~~or a slot thereon~~ for fitting at least a chip. ~~At least a~~ The chip has a back surface ~~and~~, an active surface with ~~a plurality of~~ first bonding pads, and a sidewall connecting the back surface and the active surface. The back surface and the sidewall of the chip ~~is~~ are affixed to the cavity ~~to~~ and expose the active surface. A first insulating layer is coated on both the active surface and the carrier, ~~which comprises~~ and has first ~~plating through~~ conductive holes therein. The first conductive holes are corresponding ~~connected~~ to first bonding pads ~~and via the first insulating layer~~. A multi-layer structure is on the first insulating layer, which ~~comprises~~ has conductive layout lines, second ~~plating through~~ conductive holes therein, ~~and~~ a second insulating layer thereon and exposed ball pads ~~thereon~~ in the second insulating layer. The first ~~plating through~~ conductive holes are electrically connected with the conductive layout lines, the second ~~plating through~~ conductive holes, and the exposed ball pads. A plurality of solder balls are affixed to the ball pads. ~~Such architecture integrates the redistribution and fan-out process, which simplifies the conventional process for flip-chip ball grid array.~~